



☒ L5: (18636) multi-substrat
☒ L6: (108) multi-substrate
☒ L7: (96) packag\$3 and seco
☒ L8: (665) packag\$3 and sec
☒ L9: (572) 8 and (connection conductive)
☒ L10: (202) 9 and dielectri

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DBs USPAT;EPO;JPO

Default operator: OR

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	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	<input type="checkbox"/>	<input type="checkbox"/>	US 6563224 B2	20030513	18	Three dimensional structure integrated circuit	257/778	257/777
2	<input type="checkbox"/>	<input type="checkbox"/>	US 6563184 B1	20030513	21	Single crystal tunneling sensor or switch with	257/419	257/254; 257/415;
3	<input type="checkbox"/>	<input type="checkbox"/>	US 6563111 B1	20030513	50	Integrated monolithic microfabricated electrospray	250/288	250/281; 250/282
4	<input type="checkbox"/>	<input type="checkbox"/>	US 6562545 B1	20030513	27	Method of making a socket assembly for use with a	430/313	257/179; 430/270.1;
5	<input type="checkbox"/>	<input type="checkbox"/>	US 6556420 B1	20030429	16	Wiring connection structure of laminated capacitor and	361/306.1	361/308.3; 361/313;
6	<input type="checkbox"/>	<input type="checkbox"/>	US 6556168 B1	20030429	28	Phased array antenna and its manufacturing method	342/372	
7	<input type="checkbox"/>	<input type="checkbox"/>	US 6551857 B2	20030422	22	Three dimensional structure integrated circuits	438/109	365/63; 438/107;
8	<input type="checkbox"/>	<input type="checkbox"/>	US 6549421 B2	20030415	14	Stackable ball grid array package	361/784	174/52.4; 361/735;
9	<input type="checkbox"/>	<input type="checkbox"/>	US 6544821 B2	20030408	16	Stereolithographic methods of fabricating semiconductor	438/127	438/106; 438/108;
10	<input type="checkbox"/>	<input type="checkbox"/>	US 6534395 B2	20030318	22	Method of forming graded thin films using alternating	438/627	438/643; 438/653;
11	<input type="checkbox"/>	<input type="checkbox"/>	US 6522794 B1	20030218	105	Display panel with electrically-controlled	385/4	385/10; 385/12;

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